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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/787,412	02/27/2004	Hajime Saiki	Q80149	4528

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EXAMINER	
PATEL, ISHWARBHAI B	
ART UNIT	**PAPER NUMBER**
2841	

DATE MAILED: 02/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/787,412	SAIKI ET AL.	
	Examiner	Art Unit	
	Ishwar (I. B.) Patel	2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6* is/are pending in the application.

4a) Of the above claim(s) *2 and 4* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5 and 6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Appendix "A"*.

DETAILED ACTION

1. This action is in response to the amendment filed on December 6, 2005.

Claim Objections

2. Claims 1, 3 and 6 are objected to because of the following:

Regarding claim 1, it is not clear whether "an internal conductor layer", line 8, is the same as "an internal conductor layer" as recited in line 2. For the examination purpose an internal conductor layer as recited on line 8 is considered as the same as recited on line 2.

Claim 3 depend upon claim 1 and inherit the same deficiency.

Regarding claim 6, it is not clear whether "a plurality of filled vias," line 2, are the same as "two or more via conductors", as recited in claim 5, line 15. For the examination purpose the plurality of filled vias are considered as the same as two or more vias as recited in claim 5.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. Claims 1, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson (US Patent No. 4,963,697) in view of Kawasaki (US Patent No. 6,930,258).

Regarding claim 1, Peterson, in figure 1, discloses a wiring substrate, in which a wiring stacked portion including at least one conductor layer (one of the conductor layers 105) including an internal conductor layer (internal conductor layer 105) and at least a resin layer (one of the

resin layers 101) is stacked on a principal face of a core substrate (102 with dielectric layer on top and bottom) including a substantially cylindrical through hole conductor (through hole in the core layer with plating, TH, marked on figure 1 in appendix A) in a through hole extending there through, comprising: a cover-shaped conductor (conductor 105 on the through hole, see figure 1) portion covering an end face of said through hole just over a principal face of said core substrate and connected to said through hole conductor; and an internal conductor layer (one of the conductor layers 105, above the one covering the through hole) provided on a side of the resin layer opposite said cover-shaped conductor layer, wherein a connection portion (via connecting the cover shaped conductor layer and the other conductor layers, V1, V2, V3, marked on figure 1 in appendix A) composed of at least one via conductor (one of the via, V1, V2 and V3) buried in said at least one resin layer brings said cover-shaped conductor portion and said internal conductor layer into conduction, and wherein none of said via (V1, V2, V3, marked on figure 1 in appendix A) conductors composing said connection portion are provided above said through hole (marked on figure 1 in appendix A).

Peterson does not disclose the filling material filling the hollow portion of said through hole.

Kawasaki, in figure 6, discloses a through hole (35) in the core substrate filled with a filling material (54) to have better strength of the via hole for enhanced reliability of the circuit board (column 5, line 12-27).

A person of ordinary skill in the art at the time of applicant's invention would have been motivated to fill the through hole to have a better strength and enhanced reliability of the circuit board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Peterson with the through hole filled with a filling material in order to have the through hole with a better strength and enhanced reliability of the circuit board.

Regarding claim 3, the modified circuit board of Peterson discloses all the features of the claimed invention as applied to claim 1 above but does not disclose a distance from a center axis of said at least one via conductor constructing said connection portion to an outer edge of said through hole is from 125 μm to 500 μm. However, the distance will be decided based on the routing of the conductor traces to optimize the space available to increase the trace density for connecting the components. Further, optimization of the available space will help in reducing the size of the circuit board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Peterson with a distance from a center axis of said via conductor constructing said connection portion to an outer edge of said through hole is from 125 μm to 500 μm to optimize the available space on the circuit board with better routing of the traces.

Regarding claim 5, Peterson in figure 1 discloses a wiring substrate comprising: a core substrate (102 with dielectric layer on top and bottom) including at least one through hole (through hole in the core layer with plating, TH, marked on figure 1 in appendix A) provided through said core substrate which is an insulating substrate, at least one through hole conductor

(Plating in through hole TH) which is substantially cylindrical provided on an inner circumference of said at least one through hole; a first earthing conductor layer (one of the conductors 105 on the through hole TH, see figure 1) provided on at least one principal face of said core substrate and in a shape covering an end face of said through hole and having conduction to said at least one through hole conductor; a plurality of resin layers (101) provided over said first earthing conductor layer; a transmission line (second conductor from top layer on the left in figure 1) provided between any two of said plurality of resin layers and positioned above said first earthing conductor layer; a second earthing conductor layer (first conductor layer below upper/top dielectric layer) provided over said plurality of said resin layers and in a shape containing said transmission line; and a connection portion including two of more via conductors (via connecting the conductors, V1, V2, V3 as marked on figure 1 in appendix A) buried individually in said plurality of resin layers; said two or more via conductors being provided to bring said first earthing conductor layer and said second earthing conductor layer into conduction, wherein none of said via conductors (V1, V2, V3) are positioned above said at least one through hole (see figure 1, vias V1, V2, V3 are not formed on the through hole).

Peterson does not disclose the filling material filling the hollow portion of said through hole.

Kawasaki, in figure 6, discloses a through hole (35) in the core substrate filled with a filling material (54) to have better strength of the via hole for enhanced reliability of the circuit board (column 5, line 12-27).

A person of ordinary skill in the art at the time of applicant's invention would have been motivated to fill the through hole to have a better strength and enhanced reliability of the circuit board.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the circuit board of Peterson with the through hole filled with a filling material, as taught by Kawasaki, in order to have the through hole with a better strength and enhanced reliability of the circuit board.

4. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over the modified substrate of Peterson, as applied to claim 5 above, and further in view of Shimada (US Patent No. 6,353,189).

Regarding claim 6, the combination of Peterson and Kawasaki discloses all the features of the claimed invention as applied to claim 5 above, but does not discloses the stacked via structure, in which a plurality of filled vias are concentrically contiguous to each other at a position avoiding that above said through hole. Peterson discloses the stacked via structure as shown in figure 1, avoiding the through hole, but dose not disclose them in concentric form.

Shimada, in figure 1, discloses a wiring board with via 7a-7b, formed in the concentric form for providing shielding to the transmission line 1. Further, it can be seen from the figure that space occupied by concentric via will be less than that of non-concentric via.

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of applicant's invention to provide the modified circuit board of Peterson with the filled via

concentric to each other, as taught by Shimada, in order to provide better shielding and occupy less space on the circuit board.

Response to Arguments

5. Applicant's arguments with respect to claims 1, 3, 5 and 6 have been considered but are moot in view of the new ground(s) / new explanation of rejection.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Takebe (US Patent No. 6,710,261), in figure 1, discloses a core substrate (7) with a through connector (27,27a) having plurality of conductor layers and insulating layers on both the sides of the core substrate, wherein the conductor layers are connected with via holes.

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ishwar (I. B.) Patel whose telephone number is (571) 272 1933. The examiner can normally be reached on M-F (8:30 - 5:00).

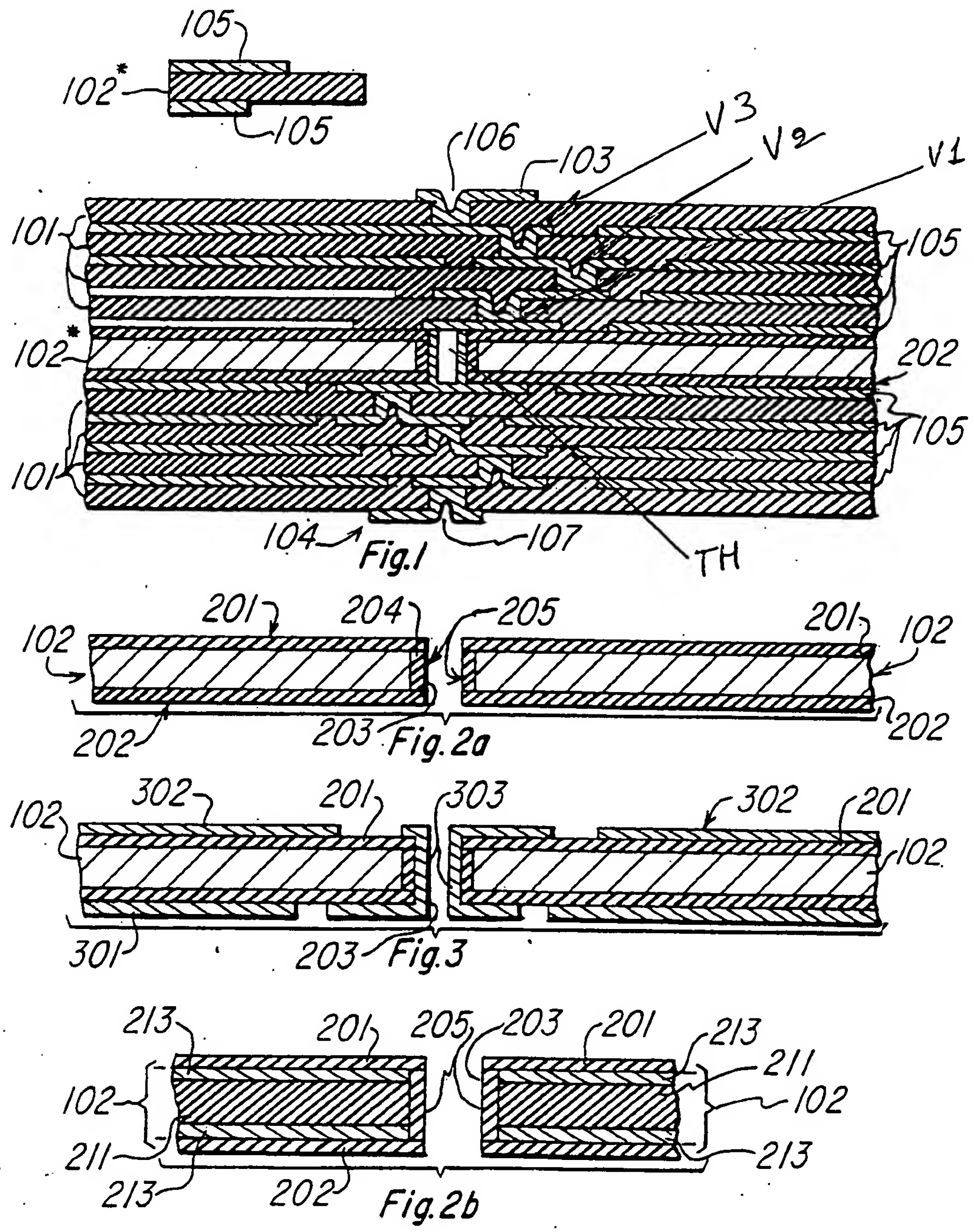
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on (571) 272 1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ishwar (I. B.) Patel
Patent Examiner
Art Unit: 2841
February 14, 2006

APPENDIX "A"

application # 10/787,412
ART UNIT: 2841



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